Analysis of Long-Term Frequency Drift in FET Oscillators

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Abstract —**This study was undertaken to analyze the long-term frequency drift observed in 11-GHz GaAs FET dielectric resonator oscillators. The analysis is based on device modeling. It is found that the dominant contributor to the long-term frequency drift is the gate-to-source channel capacitance of the GaAs FET. Results agree with the trends observed on dielectric resonator oscillators, and good correlation between theory and measured data has been achieved. The observations are general and applicable to all oscillators with GaAs FET's as active devices.**

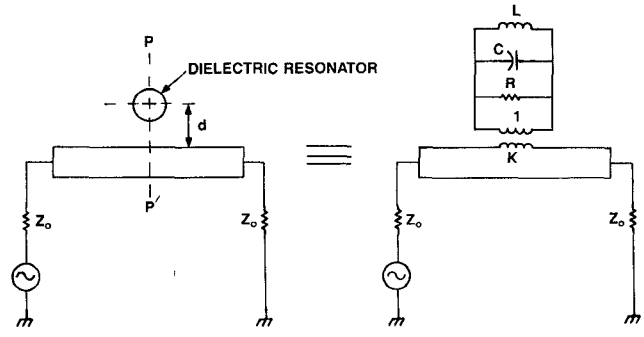
I. Introduction

DIELECTRIC RESONATOR oscillators are used in digital microwave radios as local oscillators in up and down converters. Unsatisfactory frequency stability has been observed in these oscillators. The oscillators use dielectric resonators ($\epsilon_r = 38$) for the cavities, GaAs FET's as active devices, and deliver an output power of 17.5 dBm at 11 GHz. An internal heating element is used to stabilize operation at about 80°C and reduce frequency drifts with temperature. Oscillators in the field have experienced either frequency drifts, and/or frequency jumps, causing loss of communication. These drifts were significant (20–50-kHz/day). The required frequency stability of the oscillators fell short of meeting FCC standards. The frequency of most oscillators generally moved higher, in some cases almost linearly, with time (a runaway type effect). Some units showed improvements after high-temperature burn-off and storage, but the stability targets were still not met.

An investigation of this drift mechanism was undertaken. Experimental studies of the various subcomponents (resonators, glues/epoxies, tuners, etc.) under varying temperature and humidity were undertaken along with this analytical study. *S* parameters and a GaAs FET model are used to predict analytically the long-term frequency drifts in oscillators. This method is general and can also be extended to other applications of FET's and is the first reported [1] analytical attempt to establish the long-term frequency drift behavior of oscillators.

II. Dielectric Resonator Model

The scattering parameters of several dielectric resonators were measured using an automatic network analyser (ANA) system in a fixture with a 50 ohm microstrip line, and a quartz spacer (40 mils) above the RT/duroid 6010.5 substrate. The measurement set up simulates a transmission resonance method. The model parameters of the dielectric resonator were calculated according to [2]. The equivalent circuit and the calculated parameters of the dielectric resonator are shown in Fig. 1. The model fits well and is accurate for a narrow band around the resonance frequency (e.g., 10.742–10.762 GHz) of the dielectric resonator.



PARAMETERS OF TRANS TECH DIELECTRIC RESONATOR
L = 2.059 pH
R = 673.57 ohms
C = 106.4 pF
K = 1

Fig. 1. Model of a dielectric resonator.

III. FET Model

The GaAs FET's were measured using an HP 85041A transistor fixture in an ANA system from 2 to 12 GHz. The equivalent circuit parameters were calculated using Liechtl's MESFET model [3] with some modifications for package parasitics. The calculated intrinsic and extrinsic parameters are shown in Table I. The calculated and measured *S* parameters showed an excellent agreement.

IV. FET as an Amplifier/Oscillator

First the performance of an FET as an amplifier was established using maximum available/stable gain as a criterion. Changes in maximum available/stable gain with FET parameters were calculated using the FET model. This indicated that up to +/− 10 percent variations in three critical FET parameters, C_{gs}, C_{gd}, and g_m, resulted in only a +/− 0.3-dB maximum change in the 10 to 12 dB value of available gain (Fig. 2(a) and (b)). This change in gain is of the same order as the change in gain for a 60°C change in temperature and can be easily compensat-

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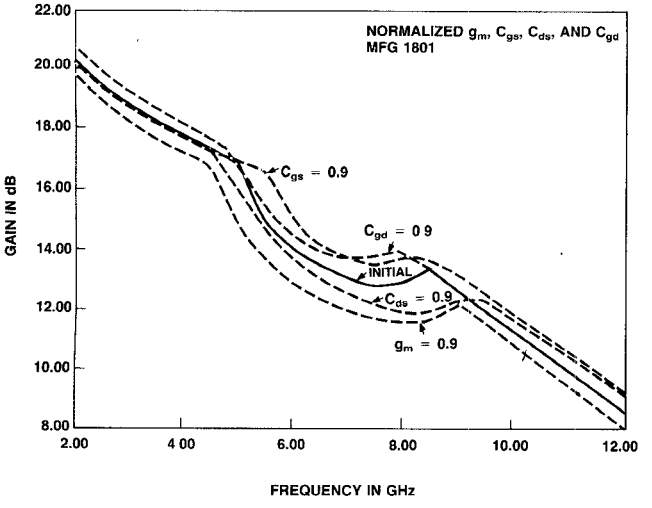
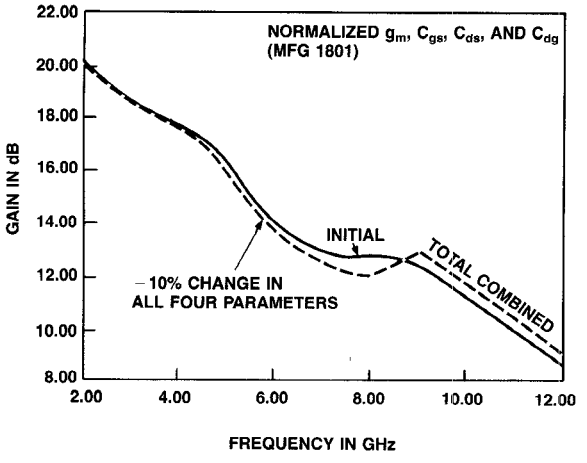
TABLE I
EQUIVALENT CIRCUIT PARAMETERS OF A MITSUBISHI MGF 1801 FET (6V/100mA)

Intrinsic Elements	
g_m	= 97 mmho
t_0	= 5.5 ps
F_{3B}	= 49.9 GHz
C_{gs}	= 1.25 pF
C_{gd}	= 0.061 pF
C_{dc}	= 0.01 pF
R_i	= 2.6 Ω
R_{ds}	= 191 Ω
R_{gs}	= 1 MΩ
Extrinsic Elements	
C_{ds}	= 0.41 pF
R_g	= 2.0 Ω
R_d	= 1.0 Ω
R_s	= 1.1 Ω
L_g	= 0.43 nH
L_d	= 0.36 nH
L_s	= 0.06 nH
C_p	= 0.29 pF
R_p	= 1.9 Ω



(a)



(b)

Fig. 2. Change of maximum available/stable gain with C_{gs}, C_{ds}, C_{gd}, and g_m.

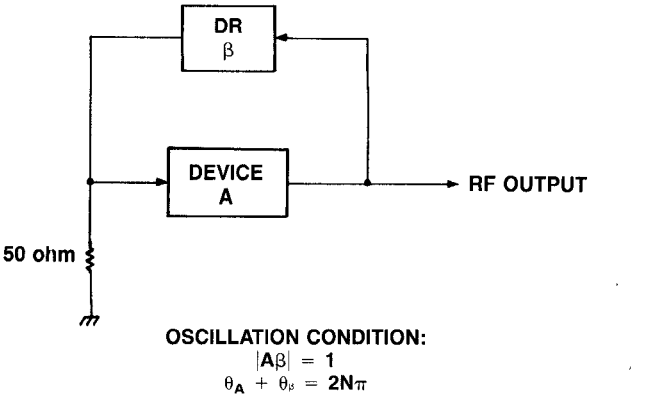


Fig. 3. Feedback circuit for DRO using FET.

ed or may not cause significant errors in specific amplifier applications.

However, the use of a GaAs FET in a high-stability oscillator (5–10 ppm) is an entirely different matter. The analysis based on FET parameters, capacitances, and transconductance showed much larger frequency drifts in oscillators than expected.

The parallel feedback DRO was realized using feedback through a dielectric resonator (Fig. 3). For the DRO to oscillate, these two conditions must be met:

$$\text{closed loop gain } |A\beta| \geq 1 \tag{1}$$

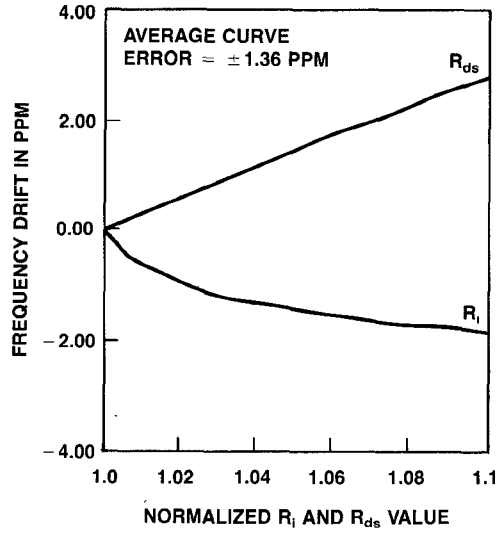
$$\text{phase of the closed loop gain } \theta_A + \theta_\beta = 2N\pi. \tag{2}$$

For the parameters in Table I and Fig. 1, oscillation at 10.75285 GHz is obtained and verified by measurement at 10.75225 GHz, showing a good agreement between computed and measured data.

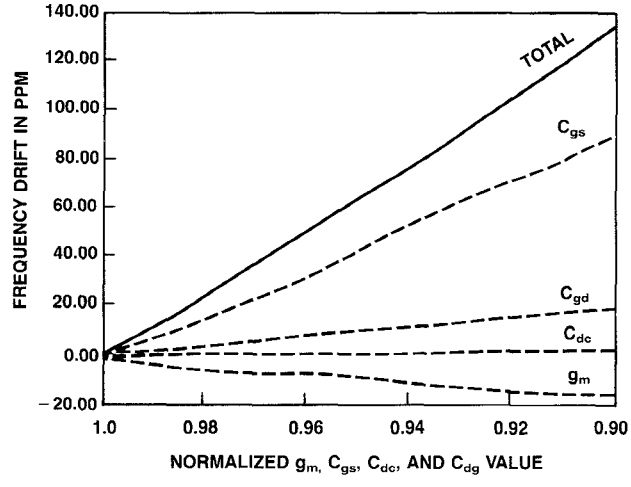
V. Oscillator Drift Analysis

Frequency drifts from all intrinsic FET parameter variations are considered. Individual parameters C_{gs}, C_{gd}, g_m, C_{dc}, R_{ds}, and R_i, were allowed to vary up to 10 percent. Such changes can be expected to occur due to device aging and the fabrication process. The frequency drifts caused by the variations of C_{dc}, R_{ds}, and R_i shown in Fig. 4(a) and (b) are insignificant (2–3 ppm for a 10-percent variation). However, the frequency drifts caused by the variations of C_{gs}, C_{gd}, and g_m are rather large (20–100 ppm for a 10-percent variation; see Fig. 4(b)). A composite long-term drift for 10-percent variations of these parameters could cause up to 135 ppm drift in frequency (Fig. 4(b)). With lower capacitance, oscillator frequency goes higher, whereas with reduced transconductance oscillator frequency goes lower. The dominant contributor to the frequency drifts is the capacitance C_{gs}. The amount of frequency drift due to C_{gd} and g_m is about the same and is small. These are the same parameters responsible for drifts in the gain of amplifiers.

From earlier reliability studies, measured time drift data for g_m and V_{gs} for various channel temperatures on a medium power FET at 12 GHz are available [4]. The g_m and V_{gs} drifts with time for different channel temperatures

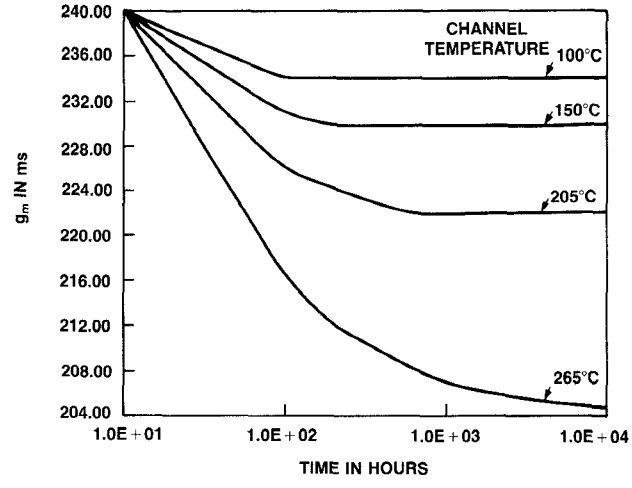


(a)

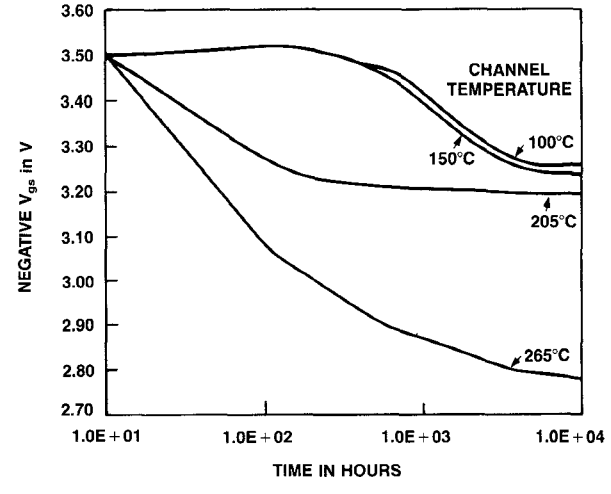


(b)

Fig. 4. Calculated DRO frequency drift using FET parameters for MGF 1801.



(a)



(b)

Fig. 5 Measured drift in g_m and V_{gs} with time for different channel temperature.

from measured data are shown in Fig. 5(a) and (b). In these figures, g_m is measured at near zero gate bias and V_{gs} is measured at constant V_{ds} and I_{ds}. The DRO FET is a smaller output power (20–23 dBm) device, and the information available is used after scaling. These data are used to establish the time behavior of the parameters.

(I) Transconductance g_m degrades to lower values with time, i.e., the gain of the device goes down.

(II) The capacitance C_{gs} over time drifts to lower values.

The behavior of g_m with time t, and channel temperature T, can be described as

$$g_m(t,T) = g_{m1}(T) + g_{m2}(T)e^{-\alpha(T)t} \tag{3}$$

where the time t is in days and channel temperature T is in °C.

The parameter $\alpha(T)$ is the channel degradation factor and can be defined as

$$\alpha(T) = \alpha_0 + \alpha_1 e^{-\beta T} \tag{4}$$

where α_0, α_1, and β are constants for a device and can be calculated by using measured data. The variables g_{m1} and g_{m2} are generally functions of channel temperature as well, and can be expressed as

$$g_{m1}(T) = g_{m10} - g_{m11}T \tag{5}$$

$$g_{m2}(T) = g_{m20} + g_{m21}e^{\gamma T} \tag{6}$$

where γ and g_{mij} are constants (found by using measured data).

One condition these $\alpha(T)$, $g_{m1}(T)$, $g_{m2}(T)$ satisfy is that at time $t = 0$,

$$g_m(0,T) = g_{m1}(T) + g_{m2}(T) = g_{m0}. \tag{7}$$

Here, g_{m0} is the transconductance generally specified by the manufactures in the data sheets. In using these relations one needs to remember that the range of T is quite large (100–300°C), and it may not always be possible to simplify exponentials by a power series expansion.

The behavior of model elements, C_{gs} and C_{gd}, can be calculated using the metal–semiconductor junction model

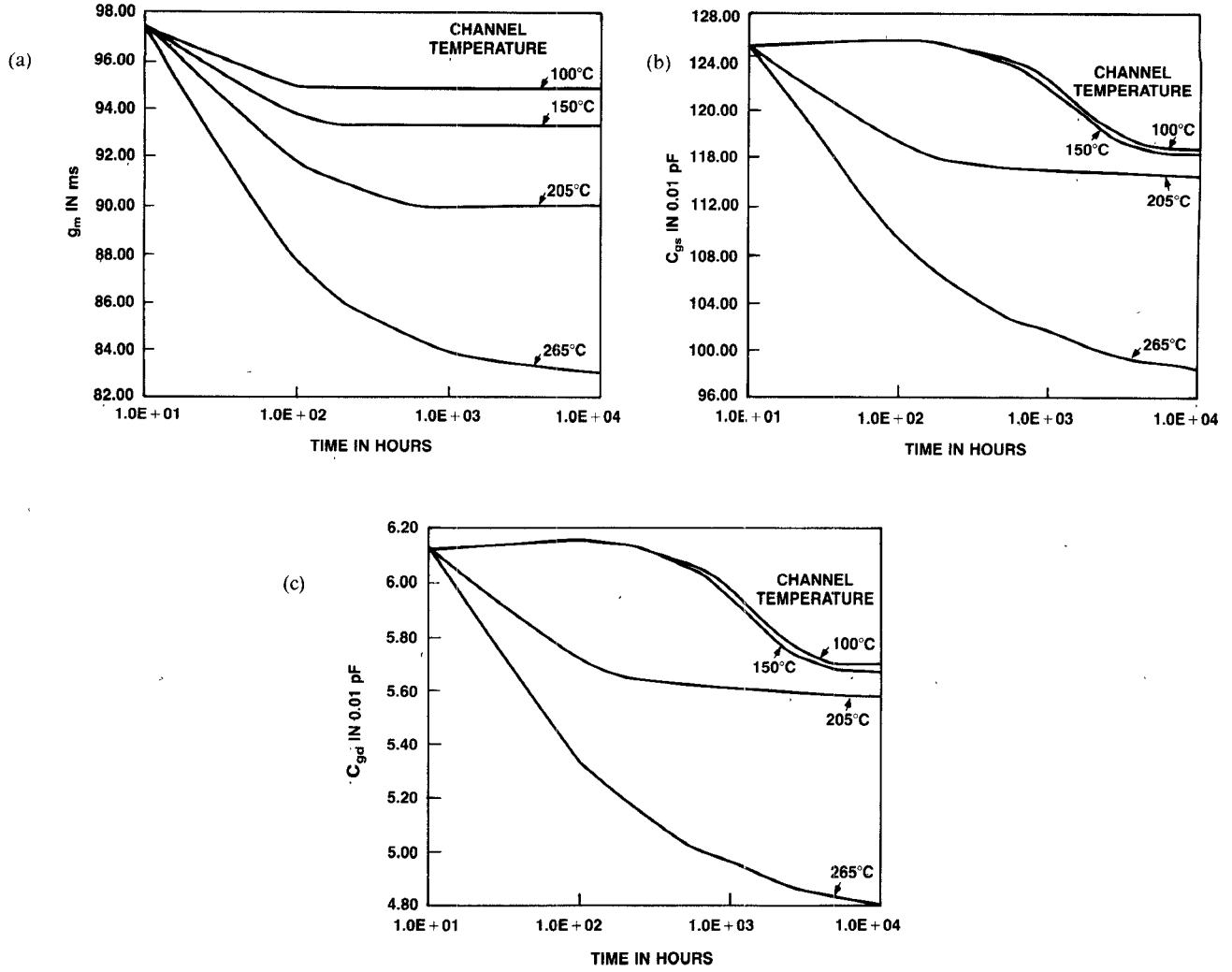


Fig. 6. Calculated drift in g_m, C_{gs}, and C_{gd} with time for different temperature (MGF1801 FET).

[5] valid for a MESFET. The depletion width W_d for a metal–semiconductor junction in a MESFET is given by

$$W_d = \sqrt{\frac{2\epsilon_s(\phi_i - V_a)}{qN_d}} \tag{8}$$

where

- ϵ_s permittivity of semiconductor $= \epsilon_r \epsilon_0$,
- ϕ_i built-in voltage,
- V_a applied voltage,
- q electron charge,
- N_d doping density.

The space charge Q_s in the semiconductor is

$$Q_s = qAN_dW_d = A\sqrt{2q\epsilon_s N_d(\phi_i - V_a)}\,. \tag{9}$$

The channel capacitance is then given as

$$C = \left|\frac{\partial Q_s}{\partial V_a}\right| = A\sqrt{\frac{q\epsilon_s N_d}{2(\phi_i - V_a)}} = \frac{A\epsilon_s}{W_d}. \tag{10}$$

For devices using hyperbolic function doping profile the following relationships are valid:

$$N_d = K_1/W_d \tag{11}$$

$$W_d = \frac{2\epsilon_s(\phi_i - V_a)}{qK_1} = K_2(\phi_i - V_a) \tag{12}$$

$$C = \frac{A\epsilon_s}{K_2(\phi_i - V_a)} = K_3/(\phi_i - V_a) \tag{13}$$

where K_1 is a constant, and $K_2 = (2\epsilon_s/qK_1) =$ constant. Also, $K_3 = A\epsilon_s/K_2 =$ constant; $A =$ area of the contact; $\epsilon_r = 13.1$ for GaAs.

In (13) V_a, the applied voltage, is related to V_{gs} and is a time-dependent parameter. Drifts of g_m and capacitors C_{gs} and C_{gd} with time for different channel temperatures are calculated using (3)–(13) for the MGF1801 FET and are shown in Fig. 6. The DRO frequency drifts with time are then calculated for different channel temperatures (Fig. 7). For devices operating at channel temperatures of 100–200°C the frequency drifts are quite large during the first few days. Then the frequency drift slows down, showing a

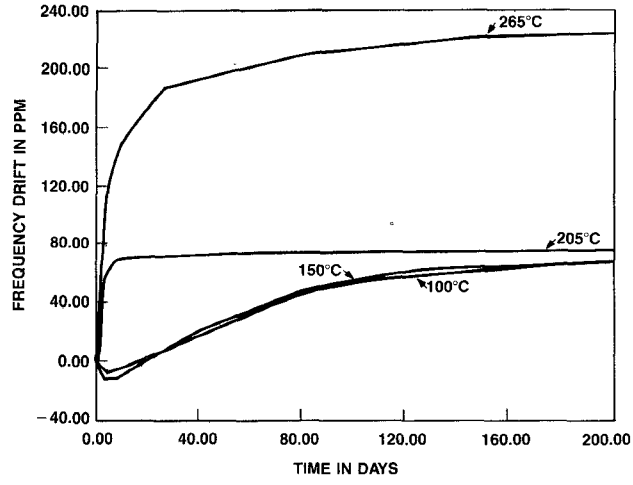


Fig. 7. Calculated long-term DRO frequency drift for different channel temperature.

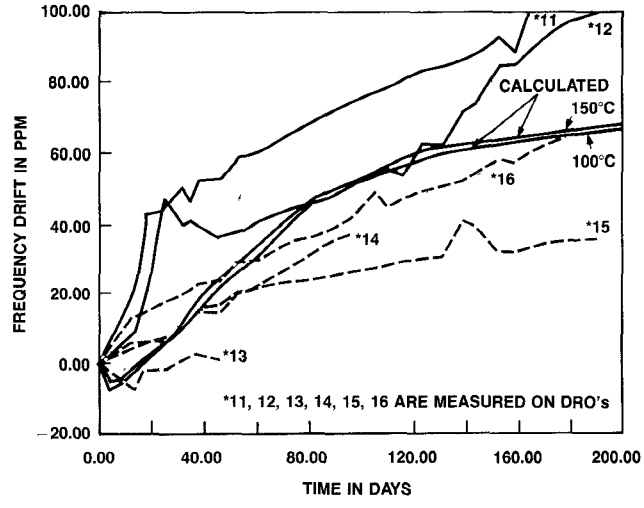


Fig. 8. Measured and calculated long-term frequency drift for several DRO's.

saturation-type effect. Furthermore, device saturation current increases initially by as much as 10 percent and then decreases steadily beyond the peak value. This causes a downward frequency drift, which steadily increases after this peak value. This effect is observed in actual oscillators and is shown in Fig. 8.

At high channel temperatures, such as 265°C, the device shows a high initial drift and continues to drift, almost like a runaway effect, and takes a long time to slow down.

VI. Experimental Results and Correlation

Based on the above analysis, the time and channel temperature model of g_m and capacitors is first verified for the large GaAs FET. The computed parameters are listed in Table II. For channel temperatures up to 265°C, the long-term behavior is accurate to about 2 percent. The device is normally biased to operate below this temperature, typically 100–115°C.

The model is used to predict the frequency drift of a GaAs FET as used in dielectric resonator oscillators. The

TABLE II
Calculated Data (Using Model) for 1-W FET

$\alpha_0 = 0.4807$	$\alpha_1 = 40.554$	$\beta = 0.033$
$g_{m10} = 256.5$	$g_{m11} = 0.17$	
$g_{m20} = 16\,107$	$g_{m21} = 0.0232$	$\gamma = 0.0253$

TABLE III
Calculated Data (Using Model) for MGF 1801 FET Used in DRO's

$\alpha_0 = 0.474$	$\alpha_1 = 6.242$	$\beta = 0.026$
$g_{m10} = 103.2$	$g_{m11} = 0.0663$	
$g_{m20} = 1.624$	$g_{m21} = 0.684$	$\gamma = 0.011$

g_m values are scaled to match the size of the device. The calculated parameters for this device are listed in Table III. The calculated long-term frequency drifts for different channel temperatures are shown in Fig. 7. Also included in Fig. 8 are the measured frequency drift curves of several DRO's (#11, #12, #13, #14, #15, #16) using MGF1801 FET. The theory predicts the behavior and general trends of long-term frequency drifts quite well, with good agreement between the calculated and measured data. DRO's #13 and #14 had catastrophic device failures in the early testing and were taken off the life test.

Analysis and experiments performed to establish other contributors to the frequency drift, such as dielectric resonator material, substrate, and glues/epoxies, indicate the associated frequency drifts are relatively insignificant compared to the contributions made by the GaAs FET. It is important to have clean resonators free from finger grease, etc., and to use good, rigid epoxies that can withstand operation at elevated temperatures.

The decrease in gate-to-source capacitance C_{gs} is the main cause of long-term frequency drifts in FET's. Although it shows that the 5–10 days of aging would improve the initial abrupt frequency drifts, one has to bias the device carefully. For devices biased at or close to the limit of their power output capability, the degradation of channel capacitance is large. Such devices would continue to drift excessively for a long time. This behavior has indeed been observed in some field units.

VII. Conclusions and Suggestions

From the above analysis, it is possible to predict the long-term drift behavior of GaAs FET–type oscillators. For the specific DRO case, it indicates that to achieve a high stability of better than 20 ppm in long-term frequency drift, the device parameters should change no more than 1.5 percent. A 10-percent change is related to a 2–3-percent change in S parameters.

Since the device model parameters change with the size of the FET and manufacturing process used by the suppliers of these FET's, one could expect to see "device-specific" and different frequency drifts and rates over time. Scaling can be used to account for the size; however, process-related differences are hard to account for. One has to establish the frequency drifts for process-related changes by characterizing the particular devices, which

may not even be possible due to the accuracy limits of the currently available measurement instruments. Changes of the order of 0.3–0.5 percent in S parameters are at the limits of the measurement accuracy of the HP8510C automatic network analyzer system.

One very important conclusion can be drawn: all FET's drift; however, the drift mechanism is aggravated if the device is used close to its maximum power output capability. Such drifts are insignificant in amplifier applications but are very strongly reflected in oscillators, with serious consequences.

One way to reduce the frequency drift phenomenon and still use GaAs FET's at high microwave frequencies is by using FET's with larger power capability. Properly biased, to deliver output powers 8–10 dB lower than the maximum power output capability of the device, good, highly stable oscillators have been realized. Larger devices, however, consume more dc power, are costly, and require a good heat sink to maintain a reasonable channel temperature.

As an alternative approach, one can use a properly biased, somewhat smaller device to design the oscillator and use amplifiers to amplify the oscillator output to more desirable higher signal levels. This approach could be cost-effective and quite beneficial in some applications and provides load isolation along with higher power from the oscillators.

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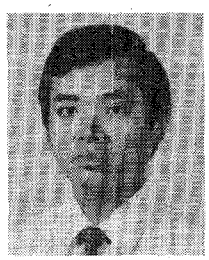

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